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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,597	11/20/2001	Xiao-Dong Yang	03226.102001;P5991	1542

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ROSENTHAL & OSHA L.L.P.  
Suite 4550  
700 Louisiana  
Houston, TX 77002

EXAMINER

DOAN, NGHIA M

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/989,597	YANG ET AL.	
	Examiner Nghia M Doan	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 20 November 2001.  
 2a) This action is FINAL.                  2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-19 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-19 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 11/20/2001 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
     If approved, corrected drawings are required in reply to this Office action.  
 12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All b) Some \* c) None of:  
 1.) Certified copies of the priority documents have been received.  
 2.) Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3.) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.  
 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
 a) The translation of the foreign language provisional application has been received.  
 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.<br> | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

1. In response to the communications dated 11/20/2001, claims 1-19 are active in this application.

**Claim Rejections - 35 USC § 102**

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1b, v5

3. Claims 1, 4, 6, 9, 11, 13, 15, 17, and 19 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. patent No. 5,610,833 to Chang et al..

4. Referring to claims 1, 6, 15 and19, Chang et al. disclose a method for creating a wire load model, comprising:

creating an interconnect configuration (figure 1a, block 100 and110);

running a field solver to generate parasitic information for the interconnect configuration (figure 1a, block 112);

storing the parasitic information in an accessible format (figure 1a, block 402);

and

running a curve-fitting engine to create the wire load model, wherein running the curve-fitting engine is dependent on the parasitic information (figure 1a, block 212 and figure 2c).

5. Referring to claim 11, Chang et al. disclose the computer system, comprising:
  - a memory for storing a worksheet known as model of a circuit (column 12, lines 51- 56, Table 6);
  - a processor for creating a wire load model, wherein the processor establishes an interconnect configuration for the circuit (column 13, lines 47-51 and Table 6);
  - a field solver known as a batch mode for determining parasitic information for the interconnect configuration (figure 1a, block 100, 114 and column 3, lines 49-55); and
  - a curve-fitting engine that uses the parasitic information to generate the wire load model (figure 2c).
6. Referring to claim 16, Chang et al. disclose the method wherein generating parasitic information uses a field solver or a batch mode (figure 1a, column 19, lines 61-63).
7. Referring to claim 4, 9, 13, and 17, Chang et al. disclose the method wherein the curve-fitting engine is a non-linear curve-fitting engine (figure 2c).

**Claim Rejections - 35 U.S.C. § 103**

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 2, 7, and 12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al.

10. Referring to claims 2, 7 and 12, Chang et al. disclose wherein a range of widths and spacings for an interconnect configuration can be applied to multiple layout parameters, such as line width, line length, inter-line spacing, and conductor thickness (column 8, lines 38-40). These layout parameters are user adjustable (column 9, lines 9-15).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the teachings from Chang et al. about the layout parameters can be adjustable as scale-up or scale-down from a minimum value. Therefore, the range of widths and spacings are chosen so that widths and spacings are either larger or smaller than the minimum width and spacing specification for the interconnect configuration.

However, those skilled in the art will recognize that such modification and variations can be made without departing from the spirit of the invention.

11. Claims 3 and 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al. in view of Jones U.S. Patent No. 5,629,860.

12. Referring to claims 3 and 8, Chang et al. disclose the method wherein a CapFile table (column 6, lines 62 and 63),

Chang et al. do not disclose a look-up table for the range of parasitic information. Jones et al. disclose an accessible format is a look-up table for the range, which is to estimate various timing delays (column 1, lines 25 and 26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teaching of Jones et al. in the inventions of Chang et al. for the purpose that the look-up tables are generated from the average effects experienced across an entire integrated circuit, which may range in different sizes. Therefore, the look-up tables are very general and assumptions about linear, variability, accuracy, and granularity adversely affect the specific design results in most cases (column 1, lines 27-34).

13. Claims 5, 10, 14, and 18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al. in view of Hammer et al. U.S. Patent No. 5,706,206.

14. Referring to claims 5, 10, 14, and 18, Chang et al. disclose the method wherein the parasitic information for group, which is interline and ground capacitances (column 6, lines 52 and 53).

Chang et al. do not disclose a group capacitance, which is including an area capacitance, a coupling capacitance, and a fringe capacitance.

Hammer et al. disclose the method wherein comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance (figure 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teaching of Hammer et al. in the inventions of Chang et al. for the purpose to calculate the parasitic capacitance attributed to an integrated circuit conductor, parasitic capacitance is an undesirable effect resulting from very close proximity of conductor (column 1, lines 42-44 and lines 48- 52).

### Conclusion

15. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia Doan whose telephone number is (703) 305-4858. The examiner can normally be reached on Monday - Friday 9:00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax numbers for the organization where this application or proceeding is assigned are (703) 746 - 9181 for regular communications and (703) 308-7722 for After Final communications.

17. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Nghia M. Doan  
Art Unit 2825  
April 23, 2002

*Matthew SIEK*

*MATTHEW SIEK*  
*Primary Examiner*